Appln. No.: Unknown Docket No.: SNDK.342US0
Title: Non-Volatile Memory and Method With Bit Line ...
Inventors: Khalid et al. Exp. Mail: EV321716491US
Filing Date: Herewith Atty. Tel: (415) 318-1160 Sheet 1 of 16

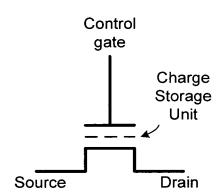


FIG. 1

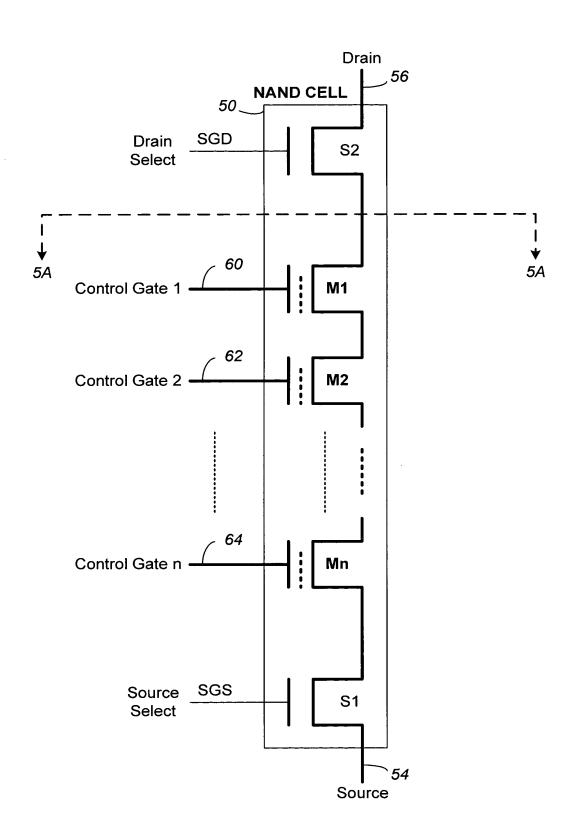


FIG. 2

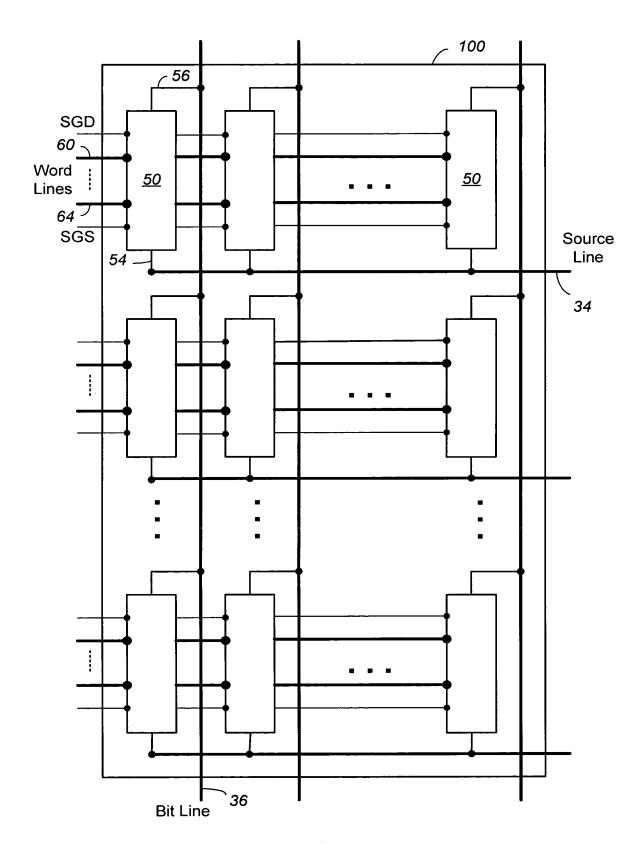


FIG. 3

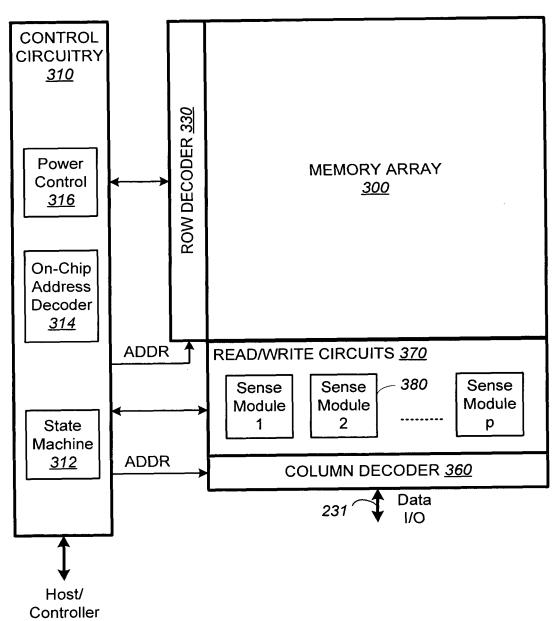


FIG. 4A

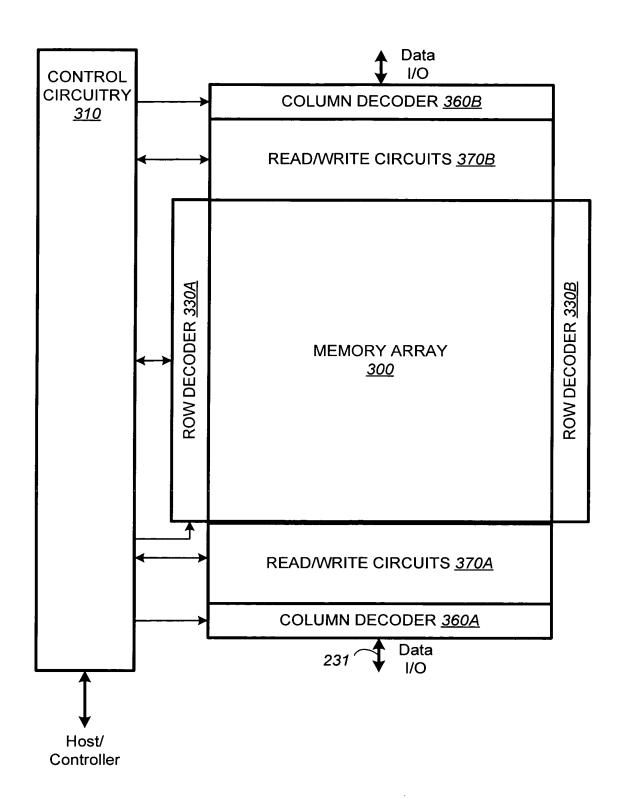


FIG. 4B

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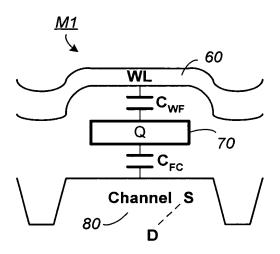


FIG. 5A

FIG. 5B

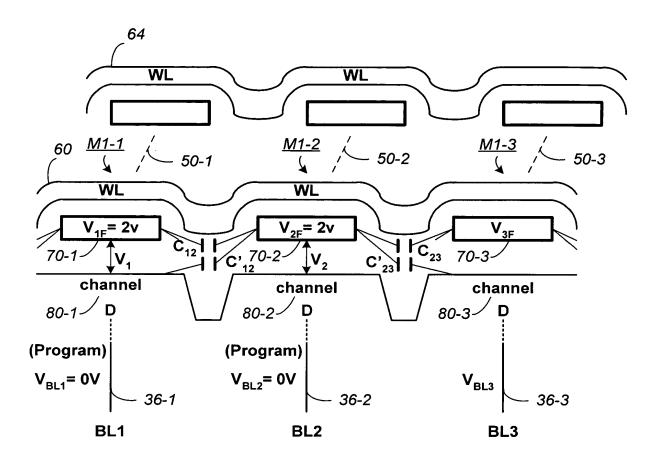


FIG. 6A

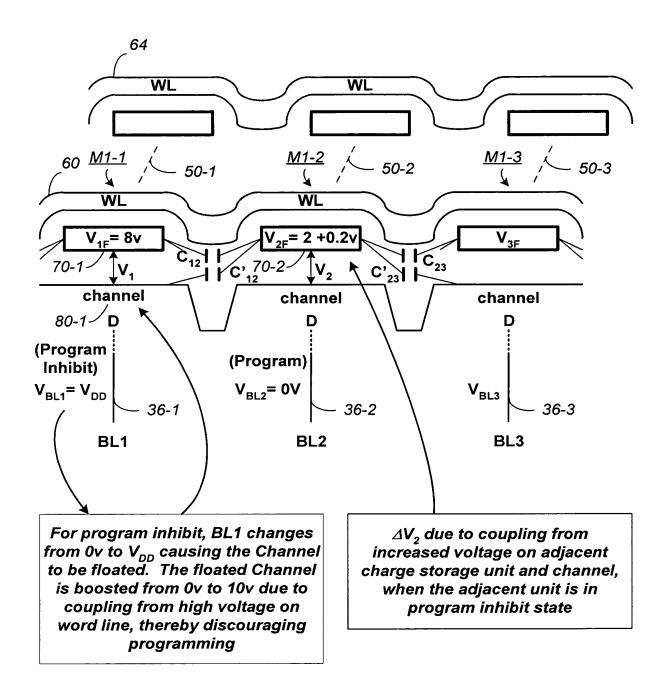


FIG. 6B

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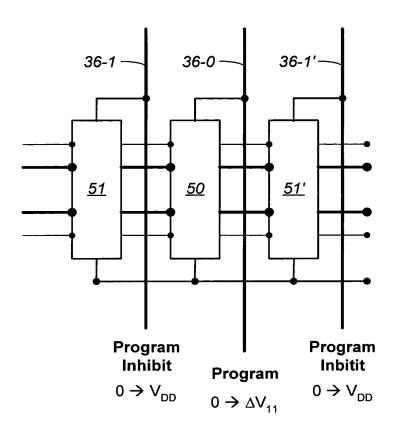


FIG. 7A

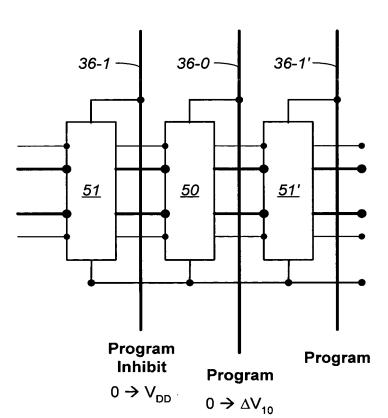


FIG. 7B

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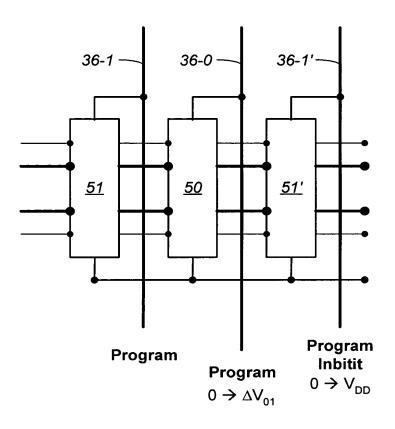


FIG. 7C

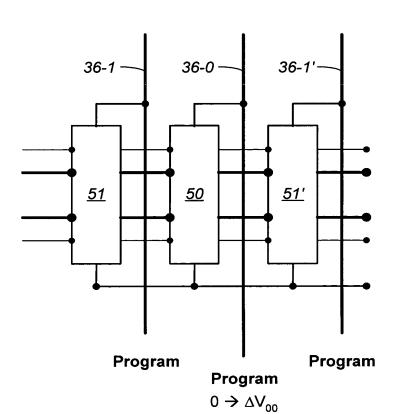
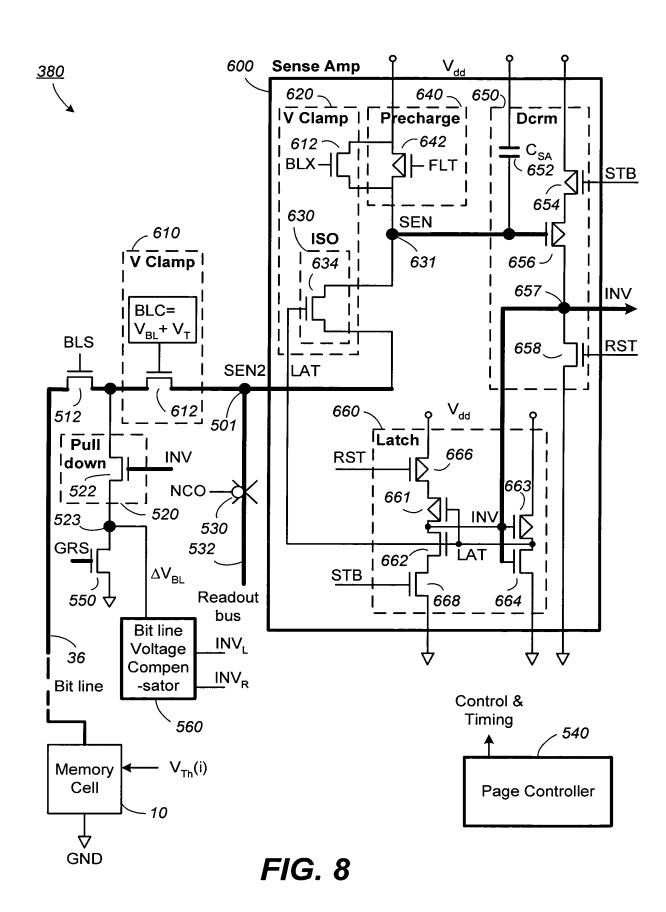


FIG. 7D



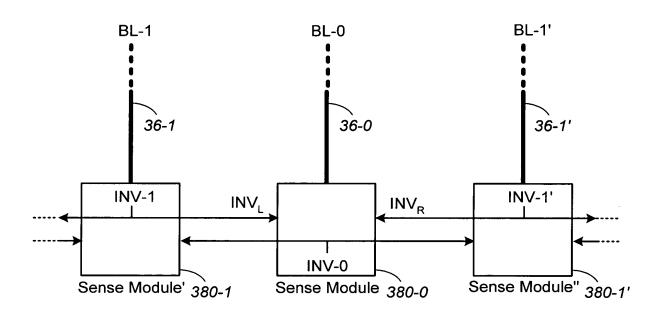


FIG. 9

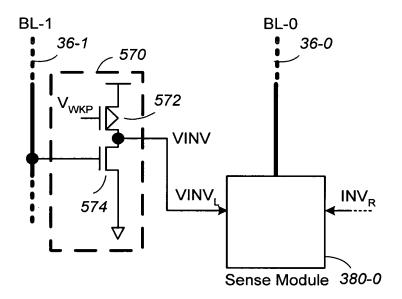


FIG. 10

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LEFT NEIGHBOR			Programming Storage Unit	RIGHT NEIGHBOR		
MODE	$INV_L$	V <sub>BL-1</sub>	Bit line Offset $\Delta V_{BL-0}$	MODE	INV <sub>R</sub>	V <sub>BL-1'</sub>
Program Inhibit	LOW	V <sub>DD</sub>	ΔV <sub>11</sub> (e.g., 0.3V)	Program Inhibit	LOW	V <sub>DD</sub>
Program Inhibit	LOW	V <sub>DD</sub>	ΔV <sub>10</sub> (e.g., 0.15V)	Program	HIGH	ΔV
Program	HIGH	ΔV	ΔV <sub>01</sub> (e.g., 0.15V)	Program Inhibit	LOW	V <sub>DD</sub>
Program	HIGH	ΔV	ΔV <sub>00</sub> (e.g., 0V)	Program	HIGH	ΔV

FIG. 11

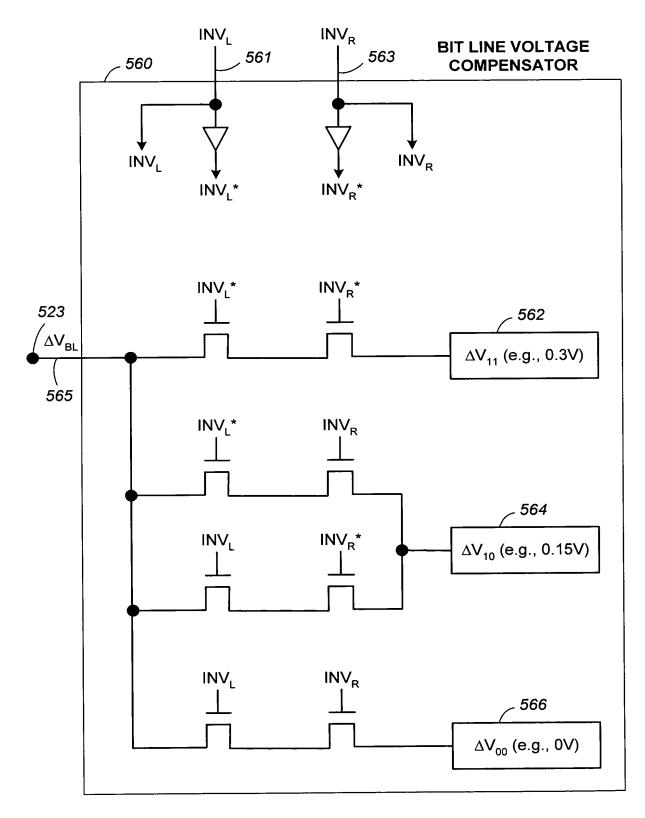


FIG. 12

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## All-bit Programming For a page of contiguous memory storage units, each unit having a charge 400 storage unit between a control gate and a channel region defined by a source and a drain, providing a bit line for each memory storage unit of the page, switchably coupled to the drain thereof and a word line coupled to all the control gates of said page of memory storage units Sensing Neighbors 410 Determining for each of those memory storage units of the page slated to be programmed whether or not its neighboring memory storage units are in a program inhibit mode Bit line Precharge with offset For those memory storage units of the page slated to be program inhibited, applying a first predetermined voltage to each of the bit lines thereof to inhibit 420 programming Applying a second predetermined voltage to each bit line of those memory 422 storage unit of the page slated to be programmed to enable programming, said second predetermined voltage for said each bit line being a function of the operation mode of its neighboring memory storage units so as to offset any perturbation therefrom Program Pulsing, Verifying & Inhibiting Applying a programming voltage pulse to said word line in order to program in parallel the memory storage units of the page, wherein those memory storage units having a bit line with said first predetermined voltage are program-430 inhibited by virtue of their floated channel boosted to a program inhibited voltage condition, and a perturbation resulted from the boosting on any neighboring programming memory storage unit is compensated by said offsetting from said second predetermined voltage Verifying if any of the memory storage units under programming has been 440 programmed to its target state Designating any memory storage units that have been verified to be slated for 450 program inhibition and any memory storage units that have not been verified to be for programming Are all memory storage units of the page verified? No , 460 Yes 470 **END**

FIG. 13

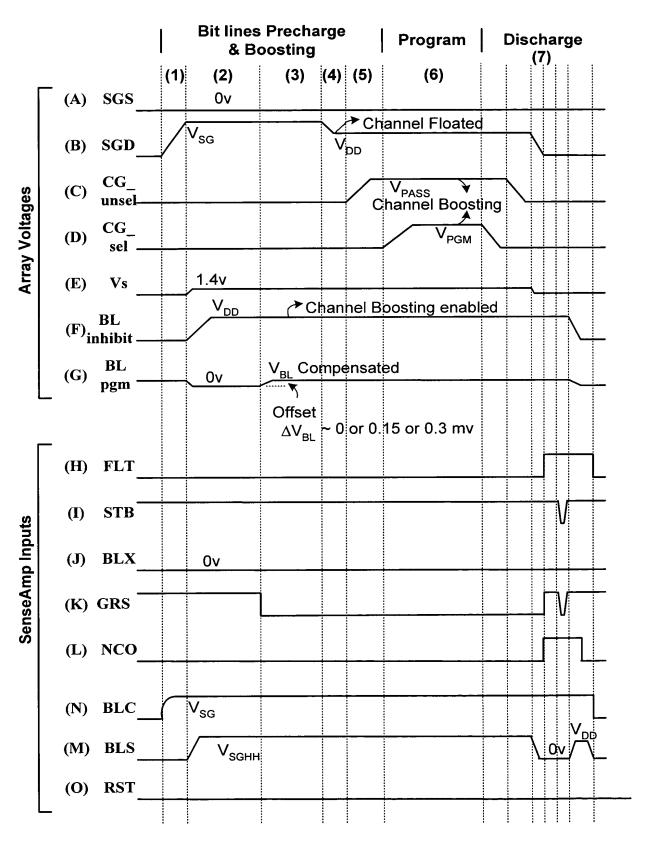


FIG. 14